VERSION WITH MARKINGS TO SHOW CHANGES MADE

31. An apparatus, comprising:
    a memory unit;
    a memory-sensing device coupled with said memory unit;
    a request queue coupled with said memory sensing device to receive more than one request to sense data in said memory unit; and
    an arbiter coupled with said memory sensing device to determine the sequence to return the data in response to the more than one request.

32. The apparatus of claim 31, further comprising a response queue coupled with said memory sensing device to store the data.

33. The apparatus of claim 31, wherein said memory unit comprises a first partition and a second partition; and said memory-sensing device comprises redundant circuitry coupled with said memory unit to sense data in the first partition and the second partition substantially simultaneously.

34. The apparatus of claim 31, wherein said request queue comprises memory to store the more than one request.

35. The apparatus of claim 31, wherein said arbiter comprises a response arbiter coupled with said memory sensing device to determine a response to the more than one request.

36. The apparatus of claim 35, wherein the response arbiter comprises a priority determiner to determine a priority of the response to the more than one request.

37. The apparatus of claim 31, wherein said arbiter comprises a request arbiter coupled with said request queue to determine a priority to sense data in response to the more than one request.

38. A system, comprising:
a memory unit;
a memory-sensing device coupled with said memory unit;
a request queue coupled with said memory sensing device to receive more than one request to sense data in said memory unit; and
an arbiter coupled with said memory sensing device to determine the sequence to return the data in response to the more than one request; and
a processor coupled with said request queue to initiate a first request of the more than one request.

39. The system of claim 38, further comprising a memory controller coupled between said request queue and said processor.

40. The system of claim 38, further comprising an input-output device.

CONCLUSION

For the aforementioned reasons, Applicant submits that claims 31-40 should be entered and are in condition for allowance. Indication of the same is respectfully requested. If Examiner has any questions concerning this application, Applicant requests Examiner to telephone the undersigned at the telephone number shown below.

Please charge any additional fees or credit any overpayment to Deposit Account No. 02-2666.

Respectfully submitted,

Date: January 7, 2002

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